PTO/SB/21 (09-04)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

		Application Number	10/626,049
		Filing Date	July 23, 2003
		First Named Inventor	Hosoya, Mutsumi
		Art Unit	2186
		Examiner Name	Unassigned
Total Number of Pages in This Submission	13	Attorney Docket Number	16869P-079400US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
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- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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- ☐ Licensing-related Papers
- ☒ Renewed Petition to Make Special
- ☐ Petition to Convert to a Provisional Application
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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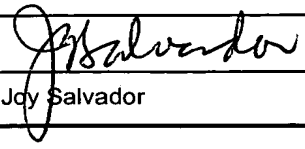
Date	January 21, 2005	Reg. No.	41,405

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
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PATENT
Attorney Docket No.: 16869P-079400US
Client Ref. No.: 310201611US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MUTSUMI HOSOYA

Application No.: 10/626,049

Filed: July 23, 2003

For: HIGH-AVAILABILITY DISK CONTROL DEVICE AND FAILURE PROCESSING METHOD THEREOF AND HIGH-AVAILABILITY DISK SUBSYSTEM

Customer No.: 20350

Examiner: Unassigned

Technology Center/Art Unit: 2186

Confirmation No.: 1442

RENEWED PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER M.P.E.P. § 708.02, VIII & 37 C.F.R. § 1.102(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Decision dated November 26, 2004 dismissing the original petition to make special, Applicants respectfully submit a renewed petition to make special the above-identified application under MPEP § 708.02, VIII & 37 C.F.R. § 1.102(d). The application has not received any examination by an Examiner.

(a) The Commissioner has previously been authorized to charge the petition fee of $130 under 37 C.F.R. § 1.17(i) and any other fees associated with this paper to Deposit Account 20-1430.

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(b) All the claims are believed to be directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicant will make an election without traverse as a prerequisite to the grant of special status.

(c) Pre-examination searches were made of U.S. issued patents, including a classification search and a computer database search. The searches were performed on or around June 17, 2004, and were conducted by a professional search firm, Kramer & Amado, P.C. The classification search covered Classes 710 (subclass 316), 711 (subclass 113), and 714 (subclasses 5 and 6). The computer database search was conducted on the USPTO systems EAST and WEST. The inventor further provided two references considered most closely related to the subject matter of the present application (see references #5 and #6 below), which were cited in the Information Disclosure Statement filed with the application on July 23, 2003.

(d) The following references, copies of which were previously submitted, are deemed most closely related to the subject matter encompassed by the claims:

(1) U.S. Patent Publication No. 2003/0084237 A1;

(2) Japanese Patent Publication No. 9-198308;

(3) U.S. Patent No. 5,724,542;

(4) U.S. Patent No. 5,615,330;

(5) Japanese Patent Publication No. 2002-041348; and

(6) Japanese Patent Publication No. 2002-242434.

(e) Set forth below is a detailed discussion of references which points out with particularity how the claimed subject matter is distinguishable over the references.

A. Claimed Embodiments of the Present Invention

The claimed embodiments relate to a high-availability disk control device that at no time, including at times of failure, leads to performance degradation in the storage system or to malfunctions in host applications.

Independent claim 1 recites a disk control device comprising a plurality of host interface modules configured to interface with a computer; a plurality of disk interface modules configured to interface with a storage device; a plurality of cache memory modules configured to temporarily store data read from or written to the storage device; and a switch network connecting the host interface modules, the cache memory modules, and the disk interface modules, the switch network comprising at least one switch. Each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules, and each of the disk interface modules is configured to execute data transfers between the storage device and the cache memory modules. Each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification within the switch network. The switch network includes a memory containing path information based on the identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules. Each of the cache memory modules is configured to monitor failure in the cache memory module and to control changing of the path information relating to the cache memory module in the memory of the switch network.

Independent claim 6 recites a disk control device comprising a plurality of host interface modules configured to interface with a computer; a plurality of disk interface modules configured to interface with a storage device; a plurality of cache memory modules configured to temporarily store data read from or written to the storage device; a plurality of resource management modules configured to store control information relating to data transfer among the cache memory modules and the host interface modules and the disk interface modules; and a switch network connecting the host interface modules, the cache memory modules, the resource management modules, and the disk interface modules, the switch network comprising at least one switch. Each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules; and each of the disk interface modules is configured to execute data transfers between the

storage device and the cache memory modules. Each of the host interface modules, the disk interface modules, the resource management modules, and the cache memory modules includes identification information providing unique identification within the switch network. The switch network includes a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, the resource management modules, and the cache memory modules. Each of the resource management modules is configured to monitor failure in the resource management module and to control changing of the path information relating to the resource management module in the memory of the switch network.

Independent claim 14 recites a disk control device comprising a plurality of host interface modules configured to interface with a computer; a plurality of disk interface modules configured to interface with a storage device; a plurality of cache memory modules configured to temporarily store data read from or written to the storage device; wherein each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules, and each of the disk interface modules is configured to execute data transfers between the storage device and the cache memory modules; wherein each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; means for connecting the host interface modules, the cache memory modules, and the disk interface modules; and means for providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules, and for changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module.

Independent claim 17 recites a disk control device comprising a plurality of host interface modules configured to interface with a computer; a plurality of disk interface modules configured to interface with a storage device; a plurality of cache memory modules configured to temporarily store data read from or written to the storage device; a plurality of resource management modules configured to store control information relating to data transfer among the cache memory modules and the host interface modules and the disk interface modules; wherein each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules, and each of the disk

interface modules is configured to execute data transfers between the storage device and the cache memory modules; wherein each of the host interface modules, the disk interface modules, the resource management modules, and the cache memory modules includes identification information providing unique identification; means for connecting the host interface modules, the cache memory modules, the resource management modules, and the disk interface modules; and means for providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, the resource management modules, and the cache memory modules, and for changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules or the resource management modules, to avoid a failed module.

Independent claim 19 recites a failure recovery processing method for a disk control device, the method comprising providing a plurality of host interface modules configured to interface with a computer; and providing a plurality of disk interface modules configured to interface with a storage device; providing a plurality of cache memory modules configured to temporarily store data read from or written to the storage device. Each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules, and each of the disk interface modules is configured to execute data transfers between the storage device and the cache memory modules. Each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification. The method further comprises connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module.

Independent claim 32 recites a disk array system for connecting to a plurality of computers via a first network. The disk array system comprises a plurality of magnetic disk devices and a disk control device connected via a second network. The disk control device comprises a plurality of host interface modules including an interface with the computers; a plurality of disk interface modules including an interface with the magnetic disk

devices; and a plurality of cache memory modules connected between the plurality of host interface modules and the plurality of disk interface modules via a switch network having at least one switch. The plurality of host interface modules, the plurality of disk interface modules, and the plurality of cache memory modules each include an ID providing unique identification within the switch network. The switch includes a memory containing path information based on the IDs for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules. The disk control device comprises means for changing the path information in the memory of the switch and the IDs.

Independent claim 38 recites a disk control device comprising a plurality of host interface modules configured to interface with a computer; a plurality of disk interface modules configured to interface with a storage device; a plurality of cache memory modules configured to temporarily store data read from or written to the storage device; and a switch network connecting the host interface modules, the cache memory modules, and the disk interface modules, the switch network comprising a processor and a memory storing a program executable by the processor. Each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules, and each of the disk interface modules is configured to execute data transfers between the storage device and the cache memory modules. Each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification within the switch network. The memory of the switch network includes path information based on the identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules. The program in the memory of the switch network includes a code module for changing the path information relating to the cache memory modules in response to an instruction from one of the cache memory modules upon detecting failure in the cache memory module.

One benefit that may be derived is that failure notification from the failure monitoring mechanism is analyzed by the path control mechanism and a forwarding table is controlled, thereby allowing the handling of flexible system structures. In large-scale disk control devices with multiple disk control subunits, failure information from multiple failure monitoring mechanisms can be collected by the path control mechanism to provide more reliable failure status analysis, thus providing reliable failure recovery processing.

B. Discussion of the References

1. U.S. Patent Publication No. 2003/0084237 A1

This reference discloses a disk array controller 1 having a plurality of disk array controlling units 1-2 and a host switch interface section 30. The disk array controlling unit 1-2 is provided with an interface (a channel interface section) 11 with the host switch interface section 30, an interface section (a disc interface section) 12 with a magnetic disc unit 5, and a cache memory section 14, in which unit a mutual connection network 21 intervenes between the channel and disc interface sections 11 and 12 and the cache memory section 14. The cache memory sections 14 of the respective disk array controlling units 1-2 are interconnected through the mutual connection network 21. It is arranged such that all of the channel interface sections 11 and the disc interface sections 12 are through the mutual connection network 21 accessible to all the cache memory sections 14. The mutual connection network 21 is arranged such that the data transfer performance thereof within a disk array controlling unit is superior to that by way of the plurality of disk array controlling units. A management table 31 is provided in the host switch interface section 30, in which table a path selection table 32 and a history information table 33 are provided, from which information table a path selection signal 40 is output to the path selection table 32, on the basis of which signal a PATH NO. 41 is selected.

In this reference, all of the channel interface sections 11 and the disc interface sections 12 are through the mutual connection network 21 accessible to all the cache memory sections 14. The host switch interface 30 is provided with the management table 31 that selects a path of the data transfer according to an address as requested by the host computer. This reference does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

2. Japanese Patent Publication No. 9-198308

This reference discloses a plurality of host computers 101, 102 connected with secondary storage devices 110, 120 through the switch 103. A cache memory 107 provided with a cache controller 104 common to the secondary storage devices 110, 120 is switch-connected to the secondary storage devices in parallel. At the time of accessing data, the host computers 101, 102 transmit data to the cache memory 107 through the switch. When a cache error occurs in the cache memory 107, a disk array management table is referred to, a port to which the secondary storage device corresponding to a logic volume in a packet is connected is specified and the secondary storage device is accessed. Data transmitted from the secondary storage device is stored in the cache memory 107 and data is transferred to the host computers 101, 102 through the switch 103.

This reference merely discloses the use of a switch and a disk array management table to improve data access performance in a data storage system. It does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

3. U.S. Patent No. 5,724,542

This reference discloses a method of controlling disk control unit. The disk control unit 30 is equipped with first and second groups each having a channel adapter 31a for interfacing the host apparatus 11; a device adapter 32a for interfacing the direct-access storage device 40a; a resource manager 35a, equipment with a control table store, for performing control related to overall resource management and processing operations, and a service adapter 36a for executing initial microprogram loading, status monitoring processing, and malfunction recovery processing; and a cache memory 33 provided so as to be shared by the first and second groups. Data commanded from the host apparatus is written in the disk

device via the cache memory or data read from the disk device is transferred to the host apparatus via the cache memory.

This reference merely discloses a cache memory through which data command from the host apparatus is written in the disk device and through which data read from the disk device is transferred to the host apparatus. It does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

4. U.S. Patent No. 5,615,330

This reference discloses a method for rapidly recovering a multiprocessor data processing system from failure of a boot disk. Each data processing unit 10, 11 in the system has a private boot disk (D0-1, D0-2 with private boot disk drive 14), and at least one shared disk (D1-1, D1-2 with shared disk drive 15). If the boot disk of one of the processing units fails, the system is temporarily reconfigured to connect a new boot disk in place of the shared disk in that processing unit. Another of the processing units is then operated to copy the contents of its own boot disk to the new boot disk.

In this reference, recovery from failure of a boot disk of one of the processing units involves temporarily reconfiguring the system to connect a new boot disk in place of the shared disk in that processing unit. It does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the

memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

5. Japanese Patent Publication No. 2002-041348

This reference relates to a communication pass through mechanism for providing network communication with high availability between a shared system resource and a client of the system resource. The system resource is provided with a control/processing subsystem with many peer blade processors. Ports of each blade processor are connected with each client/server network path and each client is connected with corresponding ports of each blade processor. Each blade processor is provided with a network failure detector to transfer beacon transmission with other blade processors via the corresponding blade processor port and a network path. Each blade processor redirects client communication to a failed port of other blade processor to the corresponding port of the blade processor by accepting that no beacon transmission is received from a failed port of other blade processor. As with other conventional approaches, this technique involves updating routing tables for each of the multiple processors, which renders failure handling time-consuming, prevents continuation of read/write tasks from the host computer, and can lead to performance degradation in the storage system and malfunction in application programs.

This reference merely discloses redirecting client communication with a failed port of one blade processor to the corresponding port of another blade processor. As discussed in the present specification at page 4, paragraph [0015], in this "conventional technology to improve reliability in disk control devices, a failure processing mechanism provides high-availability network communications between shared system resources and system resource clients." It "involves updating routing tables for each of multiple processors." "This makes failure handling time-consuming, prevents continuation of read/write tasks from the host computer, and can lead to performance degradation in the storage system and malfunctions in application programs." Present specification at page 4, paragraph [0017].

The reference does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a

memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

6. Japanese Patent Publication No. 2000-242434

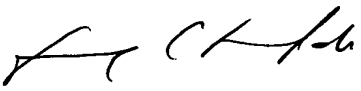
This reference discloses a storage device system constructed to correspond to the scale or request of a computer system with the goal of easily realizing the extension of a storage device system and improvement in reliability in the future. The system 1 has a plurality of subset 10 having a storage device for holding data and a controller for controlling the storage device and switch device 20 arranged between the subsets 10 and a host 30. Each switch device 20 has a managing table for holding management information for managing the configuration of the storage device system 1. According to the management information, address information contained in the frame information outputted by the host 30 is translated and the frame information is distributed to the subsets 10. In this conventional technology, a failure in one of the multiple disk array subsets is handled by updating routes and the like by interpreting packets within the switch and modifying requests to the failed sections so that their destinations are changed to redundant sections having equivalent functions.

This reference merely discloses a storage system having a plurality of subsets. As discussed in the present specification at page 4, paragraph [0016], this technique for increasing availability of disk control devices involves "a storage device system interposed between a host computer and a disk array subset and equipped with a switch performing address conversions between the two elements. In this convention technology, a failure in one of multiple disk array subsets is handled by updating routes and the like by interpreting packets within the switch and modifying requests to the failed sections so that their destinations are changed to redundant sections having equivalent functions." Such an approach requires routing changes for the host interface modules and the disk interface modules. "This makes failure handling time-consuming, prevents continuation of read/write tasks from the host computer, and can lead to performance degradation in the storage system and malfunctions in application programs." Present specification at page 4, paragraph [0017].

The reference does not teach providing a disk control device in which each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification; connecting the host interface modules, the cache memory modules, and the disk interface modules; providing a memory containing path information based on identification information for data transfer paths among the host interface modules, the disk interface modules, and the cache memory modules; and changing the path information for the data transfer paths in the memory, when a failure takes place in one of the cache memory modules, to avoid a failed cache memory module, as recited in independent claims 1, 6, 14, 17, 19, 32, and 38.

(f) In view of this petition, the Examiner is respectfully requested to issue a first Office Action at an early date.

Respectfully submitted,



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